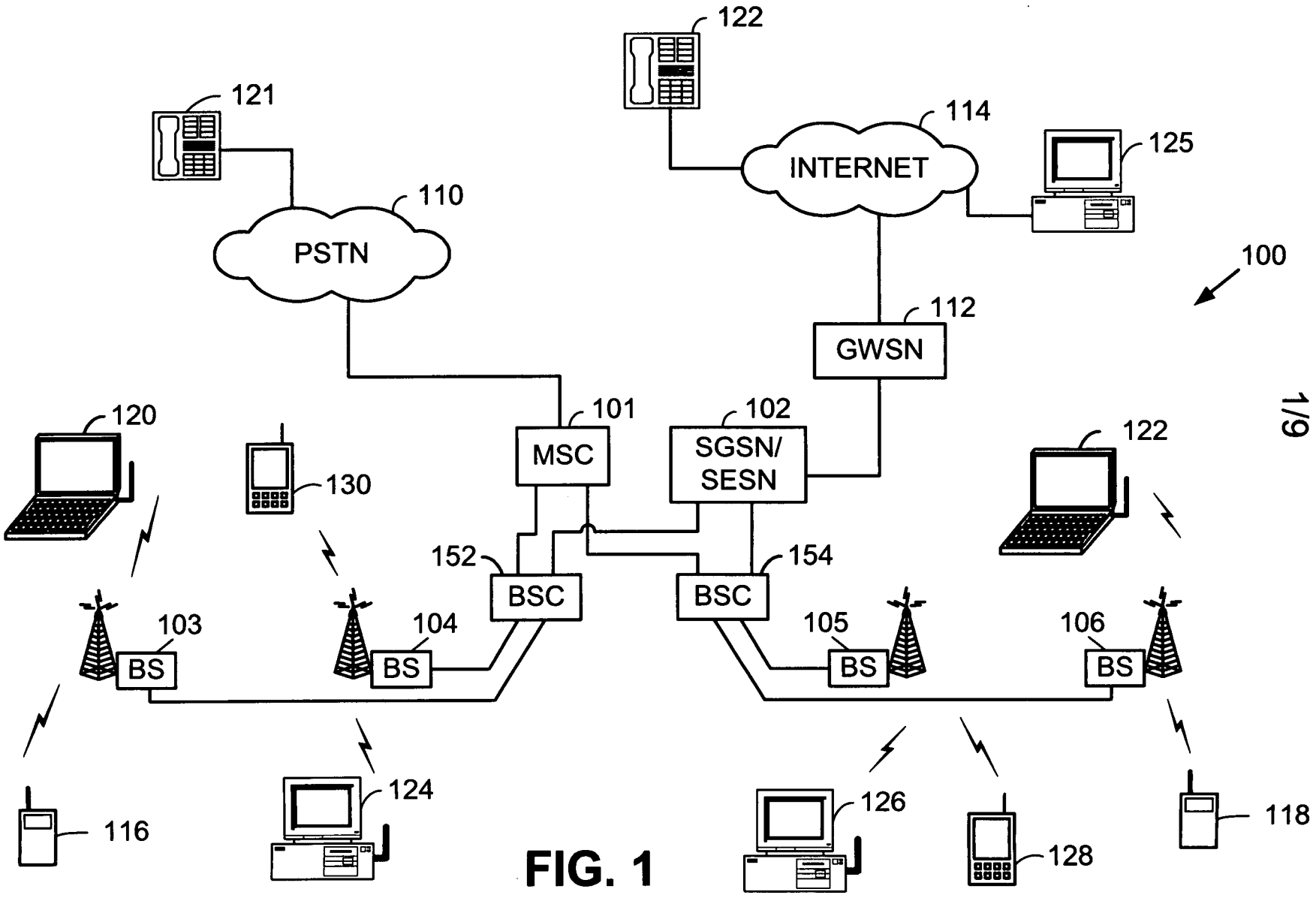

122
121
114
INTERNET
125
110
PSTN
100
112
GWSN
101
102
120
MSC
SGSN/
SESN
122
130
152
154
BSC
BSC
103
104
105
106
BS
BS
BS
BS
124
126
116
128
118

FIG. 1

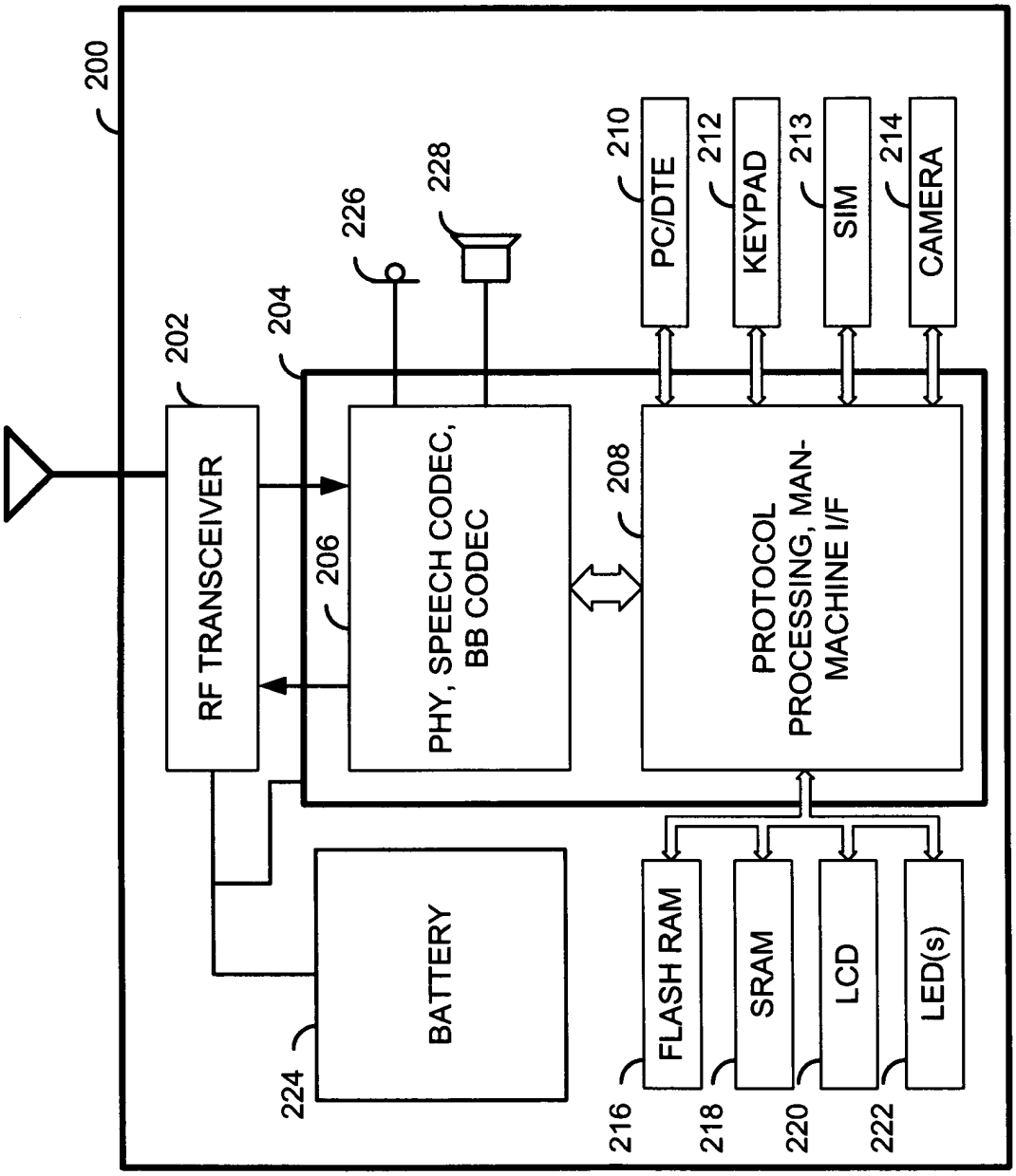

200
202
RF TRANSCEIVER
204
206
PHY, SPEECH CODEC, BB CODEC
208
PROTOCOL PROCESSING, MAN-MACHINE I/F
210
PC/DTE
212
KEYPAD
213
SIM
214
CAMERA
226
228
BATTERY
224
FLASH RAM
SRAM
LCD
LED(s)
216
218
220
222

FIG. 2

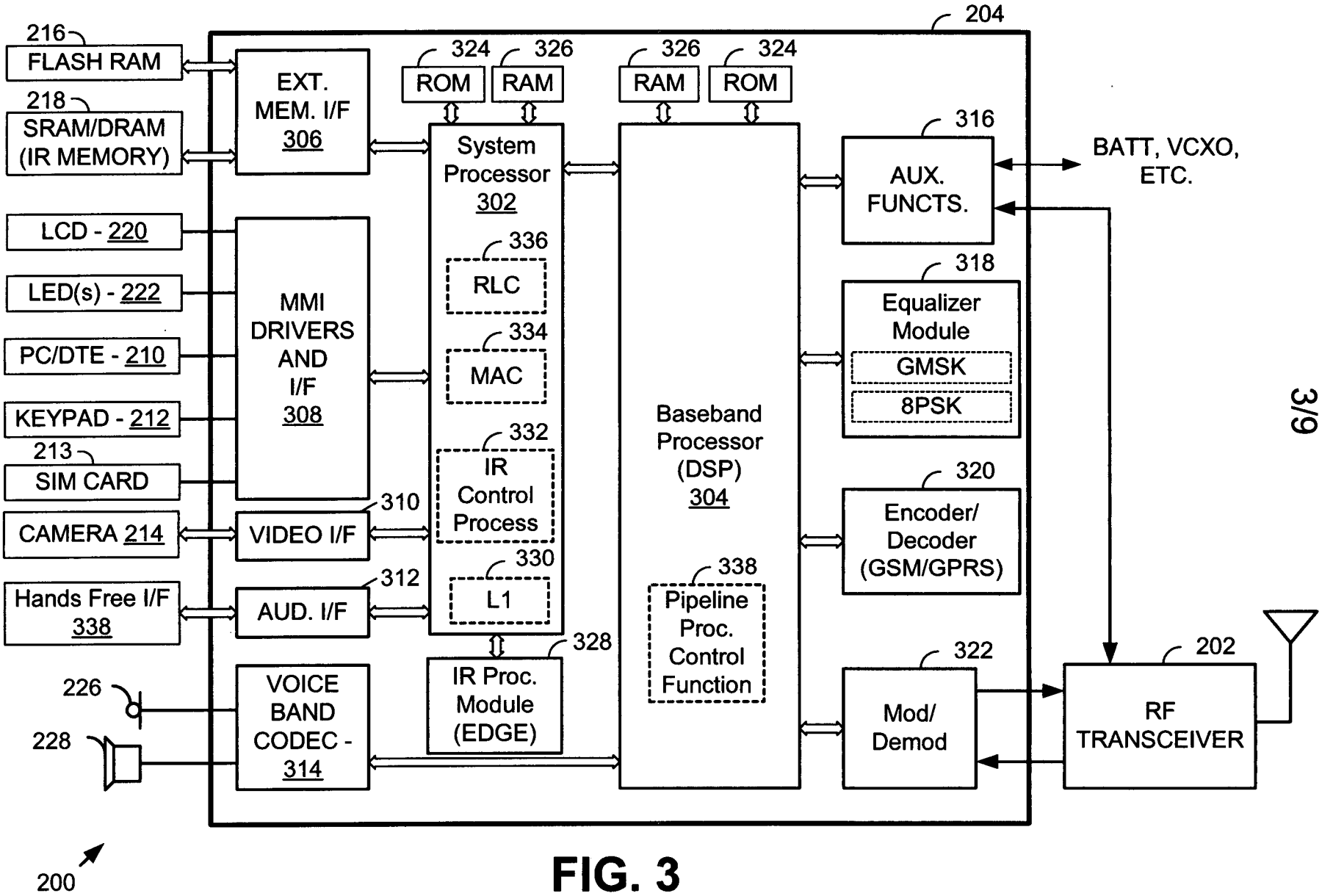

204
216
FLASH RAM
218
SRAM/DRAM
(IR MEMORY)
EXT.
MEM. I/F
306
324
ROM
326
RAM
326
RAM
324
ROM
System
Processor
302
316
AUX.
FUNCTS.
BATT, VCXO,
ETC.
LCD - 220
LED(s) - 222
PC/DTE - 210
KEYPAD - 212
213
SIM CARD
MMI
DRIVERS
AND
I/F
308
336
RLC
334
MAC
332
IR
Control
Process
330
L1
318
Equalizer
Module
GMSK
8PSK
Baseband
Processor
(DSP)
304
320
Encoder/
Decoder
(GSM/GPRS)
CAMERA 214
310
VIDEO I/F
Hands Free I/F
338
312
AUD. I/F
338
Pipeline
Proc.
Control
Function
226
228
VOICE
BAND
CODEC -
314
328
IR Proc.
Module
(EDGE)
322
Mod/
Demod
202
RF
TRANSCEIVER
200

FIG. 3

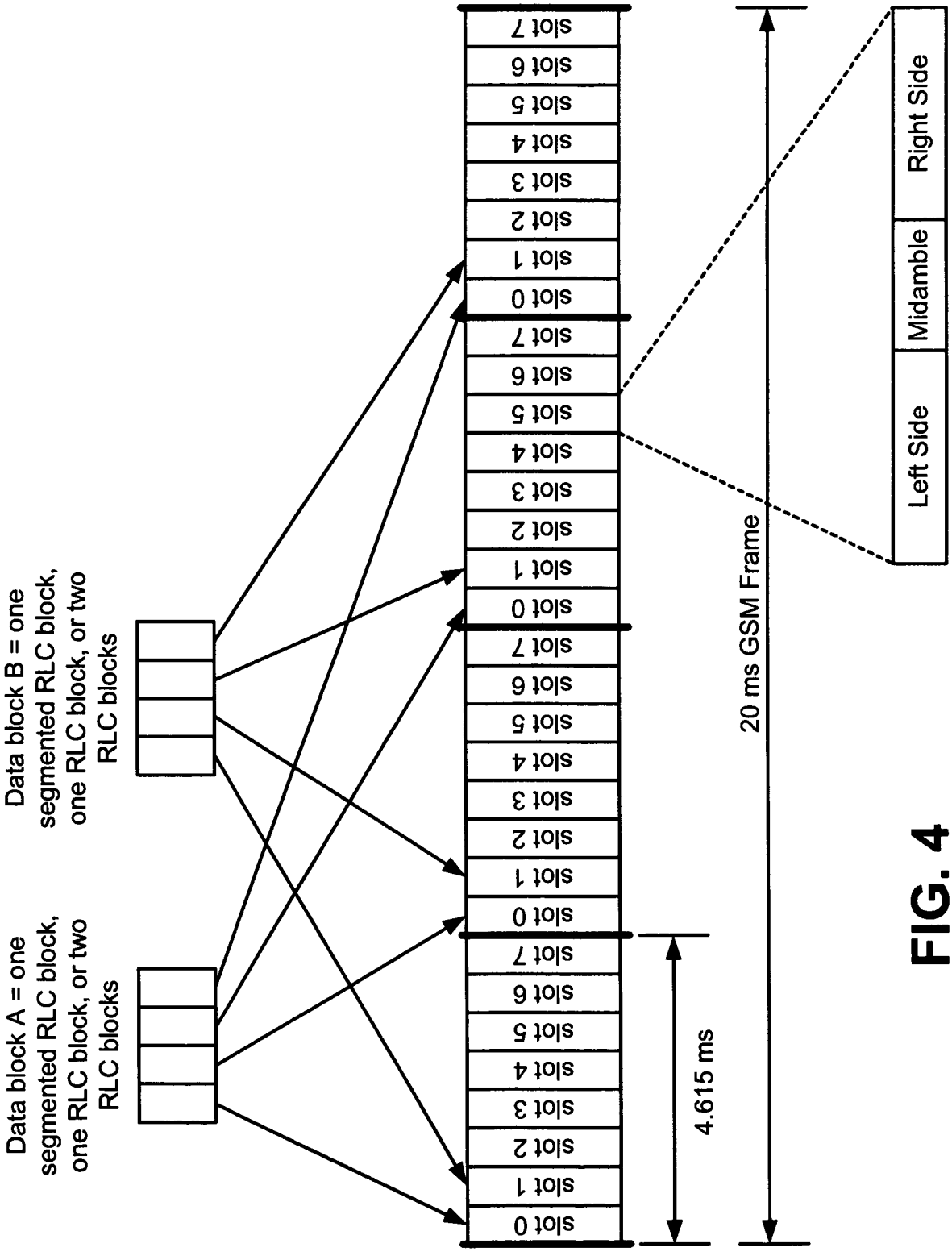

Data block A = one segmented RLC block, one RLC block, or two RLC blocks
Data block B = one segmented RLC block, one RLC block, or two RLC blocks
slot 0
slot 1
slot 2
slot 3
slot 4
slot 5
slot 6
slot 7
4.615 ms
20 ms GSM Frame
Left Side
Midamble
Right Side

FIG. 4

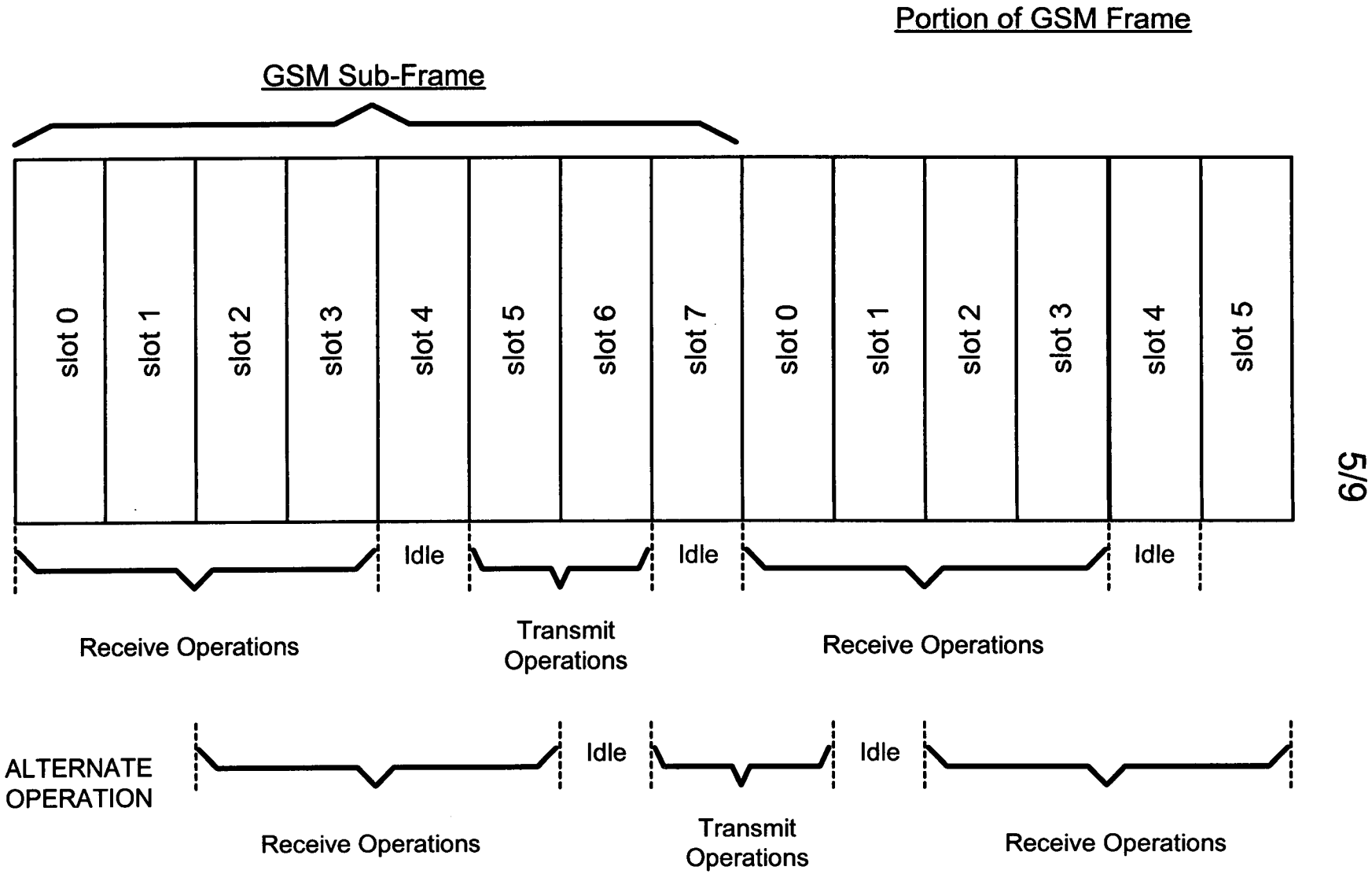

Portion of GSM Frame
GSM Sub-Frame
slot 0
slot 1
slot 2
slot 3
slot 4
slot 5
slot 6
slot 7
slot 0
slot 1
slot 2
slot 3
slot 4
slot 5
Idle
Idle
Idle
Receive Operations
Transmit Operations
Receive Operations
ALTERNATE OPERATION
Idle
Idle
Receive Operations
Transmit Operations
Receive Operations

FIG. 5

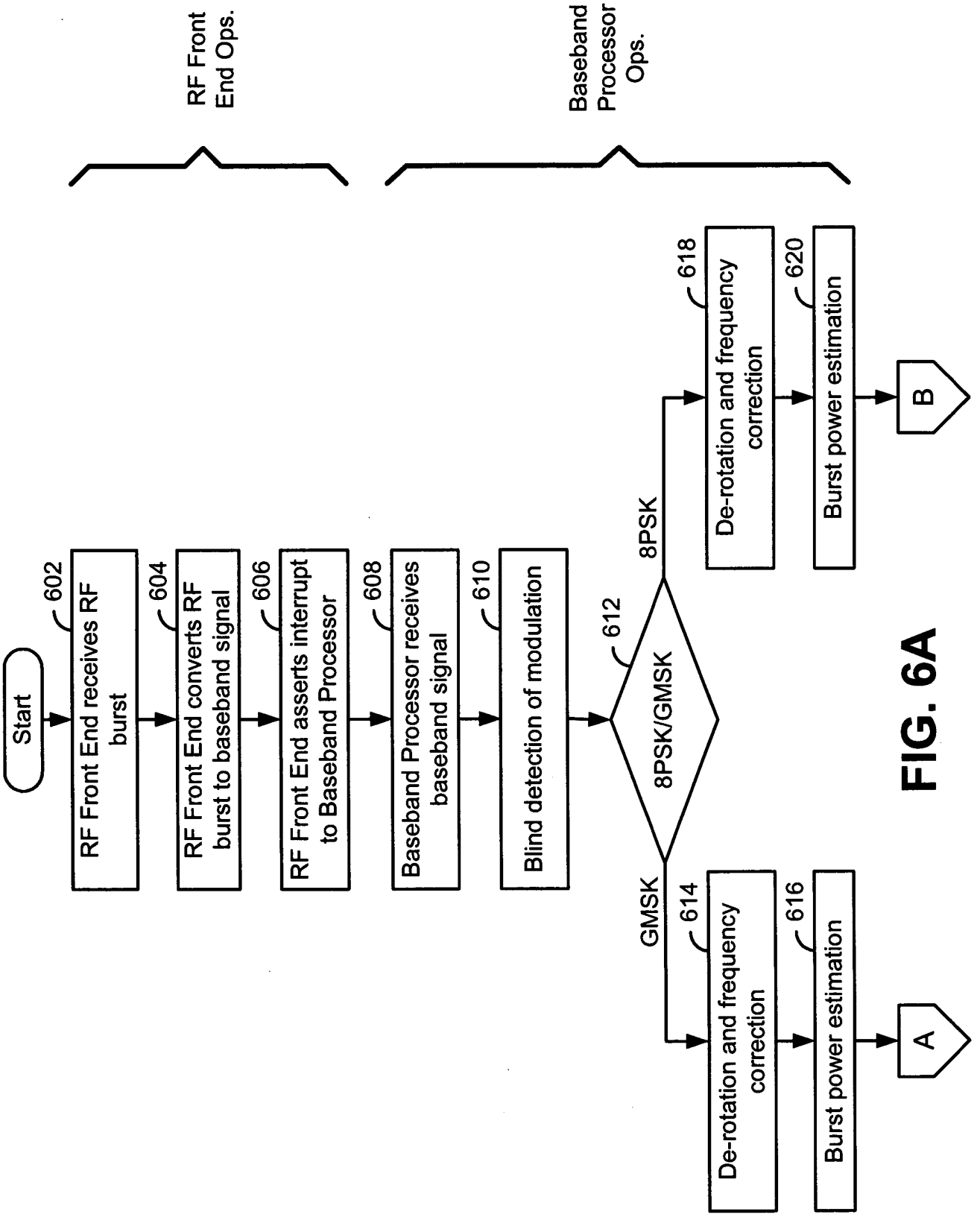

RF Front End Ops.
Baseband Processor Ops.
Start
602
RF Front End receives RF burst
604
RF Front End converts RF burst to baseband signal
606
RF Front End asserts interrupt to Baseband Processor
608
Baseband Processor receives baseband signal
610
Blind detection of modulation
612
8PSK/GMSK
GMSK
614
De-rotation and frequency correction
616
Burst power estimation
A
8PSK
618
De-rotation and frequency correction
620
Burst power estimation
B

FIG. 6A

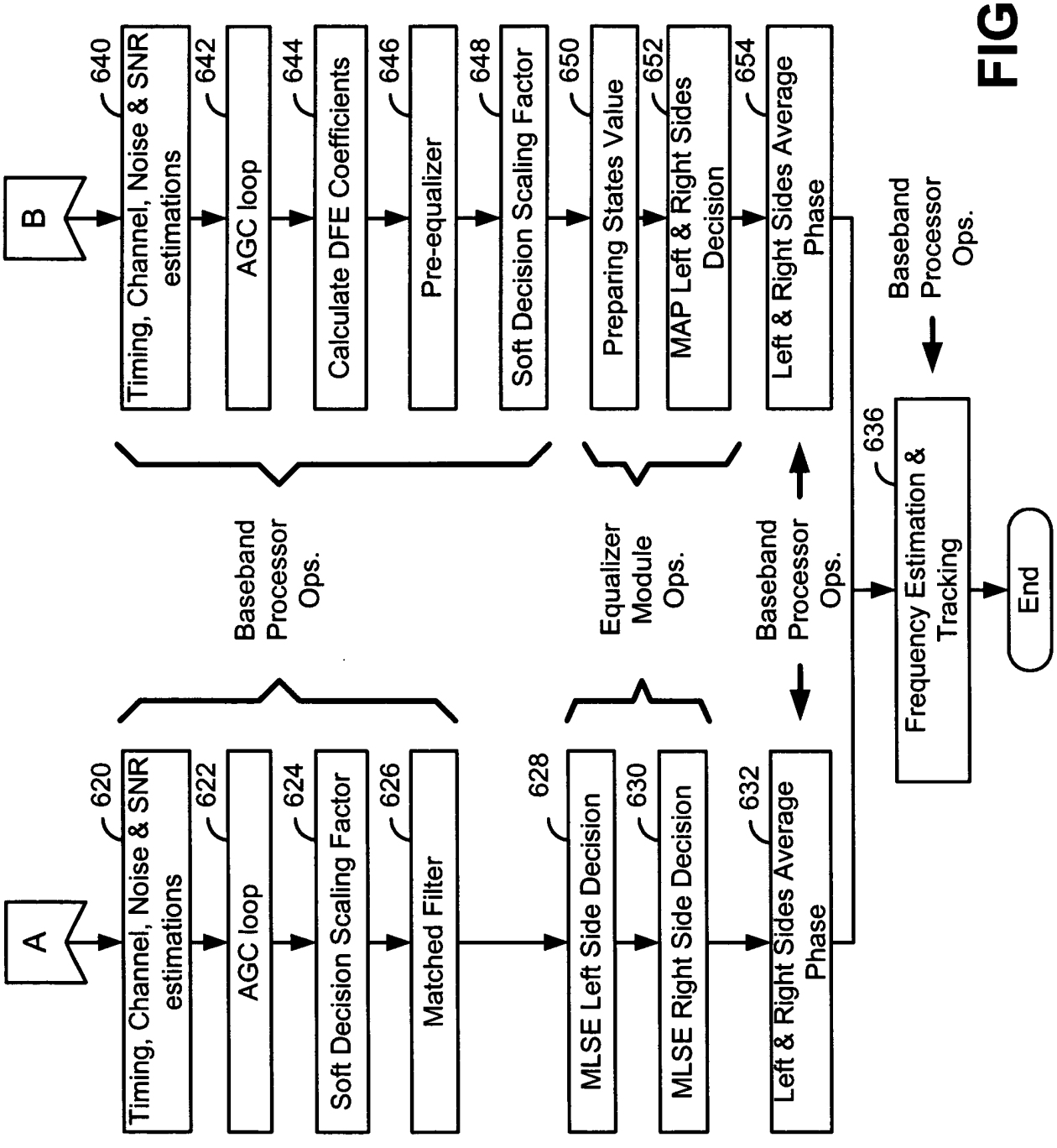

A
620
Timing, Channel, Noise & SNR estimations
622
AGC loop
624
Soft Decision Scaling Factor
626
Matched Filter
628
MLSE Left Side Decision
630
MLSE Right Side Decision
632
Left & Right Sides Average Phase
Baseband Processor Ops.
Equalizer Module Ops.
Baseband Processor Ops.
636
Frequency Estimation & Tracking
End
Baseband Processor Ops.
B
640
Timing, Channel, Noise & SNR estimations
642
AGC loop
644
Calculate DFE Coefficients
646
Pre-equalizer
648
Soft Decision Scaling Factor
650
Preparing States Value
652
MAP Left & Right Sides Decision
654
Left & Right Sides Average Phase

FIG. 6B

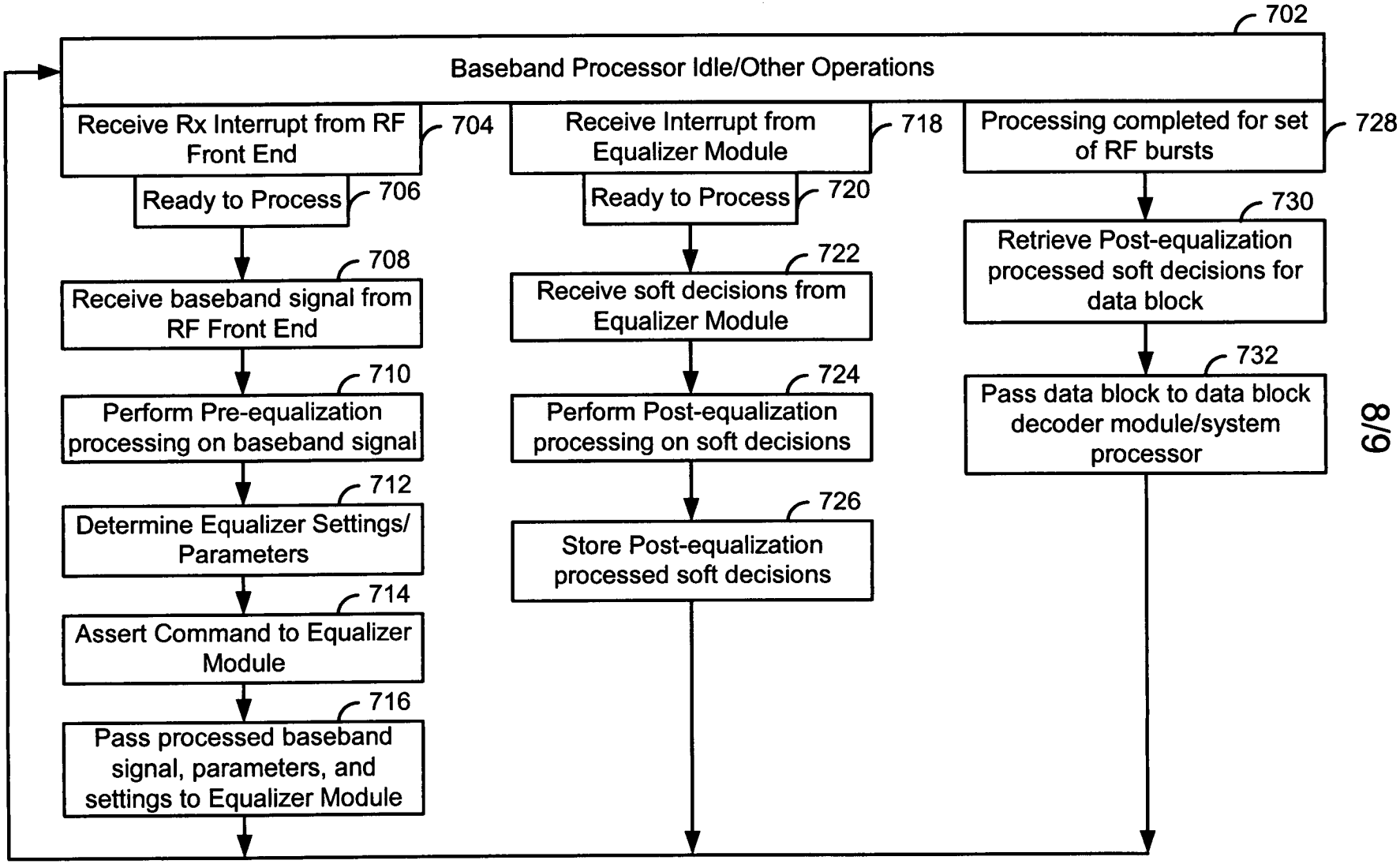

702
Baseband Processor Idle/Other Operations
Receive Rx Interrupt from RF Front End
704
Ready to Process
706
708
Receive baseband signal from RF Front End
710
Perform Pre-equalization processing on baseband signal
712
Determine Equalizer Settings/ Parameters
714
Assert Command to Equalizer Module
716
Pass processed baseband signal, parameters, and settings to Equalizer Module
Receive Interrupt from Equalizer Module
718
Ready to Process
720
722
Receive soft decisions from Equalizer Module
724
Perform Post-equalization processing on soft decisions
726
Store Post-equalization processed soft decisions
Processing completed for set of RF bursts
728
730
Retrieve Post-equalization processed soft decisions for data block
732
Pass data block to data block decoder module/system processor

FIG. 7

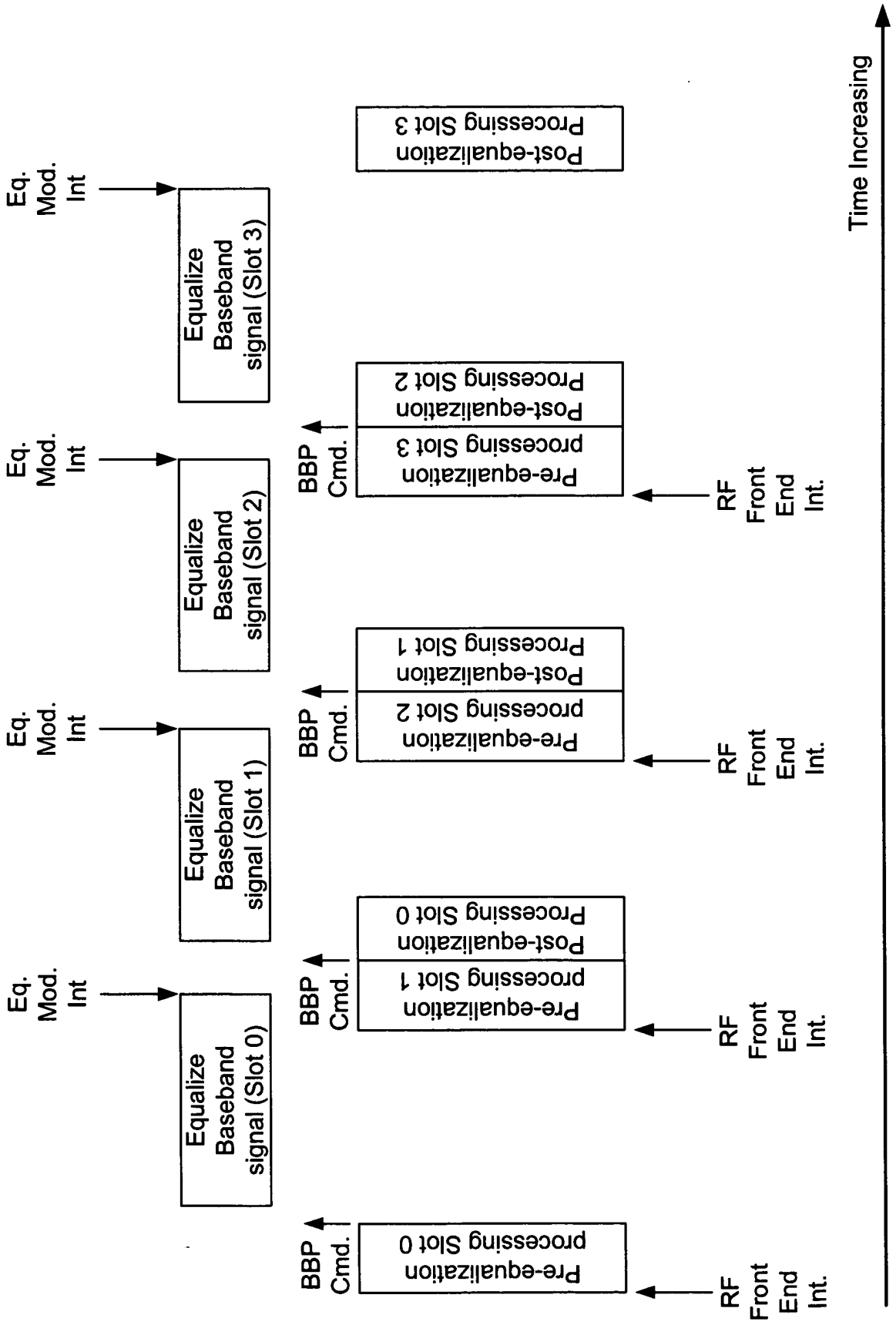

RF Front End Int.
BBP Cmd.
Pre-equalization processing Slot 0
Pre-equalization processing Slot 1
Post-equalization Processing Slot 0
Pre-equalization processing Slot 2
Post-equalization Processing Slot 1
Pre-equalization processing Slot 3
Post-equalization Processing Slot 2
Post-equalization Processing Slot 3
Eq. Mod. Int
Equalize Baseband signal (Slot 0)
Equalize Baseband signal (Slot 1)
Equalize Baseband signal (Slot 2)
Equalize Baseband signal (Slot 3)
Time Increasing

FIG. 8